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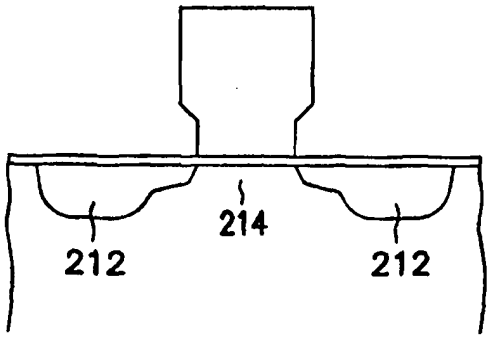

(57) Abstract

A transistor having a gate electrode with a T–shaped cross section is fabricated from a single layer of conductive material using an etching process. A two process etch is performed to form sides walls having a notched profile. The notches allow source and drain regions to be implanted in a substrate and thermally processed without creating excessive overlap capacitance with the gate electrode. The reduction of overlap capacitance increases the operating performance of the transistor, including drive current.

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TRANSISTOR WITH NOTCHED GATE

Technical Field

The present invention relates generally to integrated circuit transistors and in particular the present invention relates to metal oxide semiconductor (MOS) transistor gates.

Background

Integrated circuits transistors produced using a standard complementary metal-oxide-semiconductor (CMOS) integrated circuit fabrication process, such as MOS field-effect transistors (MOSFET), have source and drain regions, and a gate electrode. The MOSFETs are typically fabricated such that each have an n-type doped polysilicon gate electrode. The source and drain regions are typically implanted into a substrate of silicon. A channel region is defined between the source and drain regions and beneath the gate electrode. Because of overlap capacitance, gate overlap of the source and drain regions is not desired. That is, a capacitance is created between the gate and source/drain regions where an overlap exits. It is desired, therefore, to minimize this overlap.

Controlling the amount of overlap between the gate and source/drain is compounded by the need to anneal the implant regions of the source/drain to meet minimum depth requirements. One technique used to control the implant spacing between the source and drain uses spacers attached to side walls of the gate electrode. Additional fabrication steps are required to create these spacers.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a transistor which has a reduced overlap capacitance while reducing the required processing steps.

Summary of the Invention

The above mentioned problems with MOSFET's and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

In one embodiment, the present invention provides an integrated circuit transistor comprising a source, a drain, and a gate electrode formed from a single

layer and having a top region, a bottom region, and first and second opposite vertical side walls. The first and second vertical side walls have a stepped surface such that a first lateral distance between the first and second vertical side walls in the top region is greater than a second lateral distance between the first and second vertical side walls in the bottom region.

In another embodiment, an integrated circuit transistor gate electrode comprises a single layer of conductive material. The gate electrode has a top region, a bottom region, and first and second opposite vertical side walls. The first and second vertical side walls have a stepped surface such that a first lateral distance between the first and second vertical side walls in the top region is greater than a second lateral distance between the first and second vertical side walls in the bottom region.

In yet another embodiment, a method of fabricating an integrated circuit transistor is described. The method comprises fabricating a layer of conductive material, performing a first etch of the conductive material to define first and second opposite vertical side walls of a gate electrode, and performing a second etch of the conductive material to form recess regions in the first and second opposite vertical side walls. The recess regions are located at a bottom of the first and second opposite vertical side walls so that a cross-section of the gate electrode generally approximates a T-shape.

Brief Description of the Drawings

Figure 1 illustrates a transistor formed with a straight profile gate electrode and oxide spacers;

Figure 2 illustrates a "T-shaped" gate electrode formed from multiple layers of material;

Figure 3 is a cross section view of an integrated circuit transistor;

Figures 4(a)-(f) illustrate one method of fabricating the transistor of Figure 3; and

Figure 5 is a graph of transistor drain current versus over etch.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be

practiced. In the drawings, like numerals describe substantially similar components throughout the several views. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

A transistor is described herein which has a gate electrode with a "notched" profile. The notch is formed above both source and drain regions to control the location of an initial implant of source and drain extension regions. The notched polysilicon gate electrode enables an offset of the extension from the edge of the gate polysilicon to gate oxide junction. The offset provides enough lateral diffusion distance to perform an anneal operation without resulting in unwanted lateral diffusion under the gate electrode.

To more fully understand the notched gate electrode described herein, reference is made to Figure 1 illustrating a transistor 100 formed with a straight profile gate electrode 102 and oxide spacers 104. First a gate oxide layer 106 is formed on a substrate, and then a layer of gate polysilicon is deposited, masked and etched to form an electrode 102. It is noted that the lateral edges 108 and 110 of the gate polysilicon are straight. A layer of oxide is then fabricated over the gate polysilicon. The oxide is patterned and etched to form spacers 104 attached to the straight edges of the gate polysilicon. Source and drain regions 112 and 114 are then formed into the substrate using the oxide spacers to define a lateral distance between the junctions, or doped regions. An anneal operation is then performed to further vertically diffuse the source/drain regions. The annealing operation also results in lateral diffusion of the dopants under the gate polysilicon. It will be appreciated that the variables experienced in depositing, masking and etching the oxide spacers results in a variable distance between the edges of the spacers and the polysilicon edge. The lateral diffusion of the extension regions, therefore, often results in an uncontrolled overlap with the gate electrode. This overlap results in degraded performance by creating an

overlap capacitance. In addition, the extra processing steps of forming the oxide spacers are not desired.

A transistor having an alternate gate electrode is illustrated in Figure 2. The gate electrode cross section approximates a "T". That is, the top of the gate electrode is wider than the base. The transistor gate is not formed from a single layer of conductive material, but requires the deposition, patterning and etching of a second polysilicon layer 116. This transistor provides a larger interconnect conductor, but requires the multi-process steps of forming the oxide spacers and the additional gate polysilicon deposition, pattern and etch to form the top of the electrode.

To reduce overlap capacitance, while minimizing process steps, a notched gate electrode is described herein which is formed from a single layer of conductive material. Referring to Figure 3, a cross section of a fabricated integrated circuit transistor 200 is illustrated and described. The transistor includes a gate electrode 202 fabricated with notches 204. The gate electrode is separated from a substrate 250 by a layer of gate oxide 208. Source and drain regions 212 are formed (such as by ion implanting) into the substrate. The source and drain regions include extension regions 210. The area between the extension regions, and beneath the gate electrode, is referred to as the transistor body, or channel region. It will be appreciated by those skilled in the art that the notches 204 allow the diffusion of the extension regions to be a controlled distance from a vertical surface of the notch. That is, the depth of the notches defines a lateral diffusion distance which can be used during an annealing step without creating an horizontal overlap between the bottom of the gate electrode and the source/drain regions, as explained below. It will be appreciated by those skilled in the art, that the transistor illustrated in Figure 3 is not complete and that electrical contacts to the source, drain and gate are required. To focus on the present invention, these, and other optional features, have not been illustrated.

The gate electrode 202 is formed from a single layer and has a top region 203, a bottom region 205, a first vertical side wall 207 and a second opposite vertical side wall 209. The first and second vertical side walls have a stepped surface such that a first lateral distance Y between the first and second vertical side walls at the top region is greater than a second lateral distance X between

the first and second vertical side walls at the bottom region. In one embodiment, distance Y is approximately 20 nano meters larger than distance X. It will be appreciated that the difference between Y and X can vary over a wider range, including but not limited to 10 to 40 nano meters. The transistor has a general T-shaped gate in a cross section view which intersects the source and drain regions.

A description of one method of fabricating a transistor having a notched gate electrode is provided as follows, with reference to Figures 4(a)-(f). Figure 4(a) illustrates a cross-section of a semiconductor substrate 250, a layer of gate oxide 208 and a layer of material, such as doped polysilicon 252. It will be appreciated that the substrate in the region of the transistor can be isolated from adjacent circuits and doped accordingly for the type of transistor desired, as known in the art. The polysilicon layer 252 is masked and bulk etched to define the upper edges and the vertical side walls of the gate electrode 254, as shown in Figure 4(b). Once the gate oxide layer is reached, a selective etch is performed to create the notches 204 on the bottom edges of the gate electrode, see Figure 4(c). The second etch process is highly selective and does not remove much gate oxide 208. As such, there is no breakthrough of the gate oxide. The selective etch removes passivation at the polysilicon to gate oxide corner, and allows lateral etching of the polysilicon gate electrode to create the notches 204. During the selective etch process, the lateral etch rate approaches saturation to enable uniform control of the lateral undercut. Thus, the formation of the notches is close to self limiting. The selective etch is performed with the bulk polysilicon etch process, but can be considered a separate step because the etch control parameters are changed. The selective etch is a low pressure, high power etch which has a duration approximately equal to the duration of the bulk polysilicon etch, in the range of about 20 to 40 seconds.

In one embodiment, the selective etch is performed using a commercially available Hitachi M511 plasma etcher. The process is performed using the settings shown in Table 1.

Parameter	Units	Breakthrough Etch	Bulk Etch	Over Etch 1	Over Etch 2
TCR temp	deg C	5	5	5	5
EL height	mm	80	80	80	80
Pressure	Pa	0.4	0.4	0.4	1.2
RF Power	W	60	25	20	25
uW Power	W	400	400	400	400
Gas A, Cl	ccm	25	25	25	0
Gas B, O_2	ccm	3	3	3	5
Gas C, HBr	ccm	75	75	75	100
Coil 1	A	14	14	14	14
Coil 2	A	17	17	17	14
Coil 3	A	3	3	3	3
Time	sec	5	EP	24	12
He Backside	kPa	1	1	1	1
Cont Plasma	y/n	n	y	y	n

TABLE 1

The process uses a first etch, or Break through etch, to remove surface oxide. The bulk etch removes polysilicon to the gate oxide layer. The end point (EP) of this etch is based on measuring gas chemistry in the etch chamber to physically determine when all the polysilicon has been removed. The over etch 1 step straightens the polysilicon profile to forms the final profile with the above defined notches. An optional over etch 2 process can be used to remove any residual of polysilicon remaining after the over etch 1 step.

Referring to Figure 4(d), after the notched profile of the polysilicon gate is formed, a shallow implant operation is performed to form the extension regions of the source and drain. The implant is spaced laterally from the bottom of the gate electrode. That is, the top of the gate electrode patterns the shallow

implant regions by defining lateral boundaries so that the implant regions do not extend under the gate. The implant regions, therefore, do not substantially extend under the gate, and beyond vertical planes 257 and 258 defined by the side wall surfaces of the top region 203 of the gate electrode.

The extension regions of the source and drain must vertically extend into the substrate a minimum depth to reduce current spreading resistance. Thus, the shallow implant is thermally processed, or annealed, to further diffuse the implant vertically, Figure 4(e). The anneal operation also laterally diffuses the implant regions. By controlling the anneal operation, the lateral diffusion distance can be tailored to match the notch depth. As such, overlap between the gate electrode and the source/drain regions is reduced. After the thermal processing, the source and drain regions 210 extend under the gate electrode beyond the vertical planes 257 and 258. The source and drain regions 210, however, do not appreciably extend under the gate electrode beyond vertical planes defined by the interior surface of the notches 204. Finally, a deep implant is performed to form the full source and drain regions. It will be appreciated that the deep implant is performed to provide low resistance contacts. Doping of the elements and regions of the transistor is considered well known in the art, and is not discussed further herein.

Several benefits are provided by fabricating transistor gate electrodes with a notched profile. The first benefit is provided in patterning the polysilicon layer. As transistor dimensions reduce, patterning the process layers becomes more difficult. The present transistor gate allows the polysilicon to be patterned using the larger area of the top of the gate electrode, while providing a smaller gate oxide interface area. Second, the overlap capacitance of the transistor is reduce, as explained above. Figure 5 is a graph of transistor circuit performance versus over etch depth. The graph illustrates the percent improvement (increase) in oscillation frequency of a ring oscillator using notched transistors. The notch depths were created using increased etch times. The first sample (a) did not contain notches, while the remaining samples had increasing notch depths. Sample (e) had a depth of approximately 15-20 nm, and sample (I) had a depth of approximately 20-25nm. A ring oscillator was used to illustrate the performance increase attributed to the reduced capacitance of the transistors,

with other variable remaining constant. It can be seen that as the depth of the notches increase, the oscillator performance also increases. This performance increase has limitations, and will plateau or decrease as the notch depth continues to increase. Thus, the performance of the last sample (j) begins to decrease due to an increased resistance between the extension regions which do not fully reach the gate polysilicon (negative over lap).

Conclusion

A method of reducing overlap capacitance in an integrated circuit transistor has been described herein. The method comprises forming a transistor gate electrode, having a T-shaped cross section, from a single layer of material using an etching process. In one embodiment, a two process etch is performed to form side walls having a notched profile. The notches allow source and drain regions to be implanted and thermally processed without creating excessive overlap capacitance. The reduction of overlap capacitance increases the operating performance of the transistor.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An integrated circuit transistor comprising:

a source;

a drain; and

a gate electrode formed from a conductive layer and having a top region, a bottom region, and first and second opposite vertical side walls, the first and second vertical side walls have a stepped surface such that a first lateral distance between the first and second vertical side walls in the top region is greater than a second lateral distance between the first and second vertical side walls in the bottom region.

2. The integrated circuit transistor of claim 1 wherein the source extends laterally under the gate, and beyond a vertical plane defined by the first vertical wall surface at the top region.

3. The integrated circuit transistor of claim 2 wherein the source is implanted in a substrate such that it does not extend laterally under the gate, beyond a vertical plane defined by the first vertical wall surface at the top region.

4. The integrated circuit transistor of claim 3 wherein the source is thermally processed, after being implanted, to laterally diffuse the source under the gate, and beyond a vertical plane defined by the first vertical wall surface at the top region.

5. The integrated circuit transistor of claim 1 wherein the drain extends laterally under the gate, and beyond a vertical plane defined by the second vertical wall surface at the top region.

6. The integrated circuit transistor of claim 5 wherein the drain is implanted in a substrate such that it does not extend laterally under the gate, beyond a vertical plane defined by the second vertical wall surface at the top region.

7. The integrated circuit transistor of claim 6 wherein the drain is thermally processed, after being implanted, to laterally diffuse the drain under the gate, and beyond a vertical plane defined by the second vertical wall surface at the top region.

8. The integrated circuit transistor of claim 1 wherein the gate electrode is formed from the single layer using a bulk etch process and a selective etch process.

9. The integrated circuit transistor of claim 1 wherein the first lateral distance is greater than the second lateral distance by approximately 20 nano meters.

10. An integrated circuit transistor gate electrode comprising:

a single layer of conductive material, the gate electrode has a top region, a bottom region, and first and second opposite vertical side walls, the first and second vertical side walls have a stepped surface such that a first lateral distance between the first and second vertical side walls in the top region is greater than a second lateral distance between the first and second vertical side walls in the bottom region.

11. The integrated circuit transistor gate electrode of claim 10 wherein the gate electrode is formed from the single layer using a bulk etch process and a selective etch process.

12. The integrated circuit transistor of claim 10 wherein the first lateral distance is greater than the second lateral distance by approximately 20 nano meters.

13. A method of fabricating an integrated circuit transistor, the method comprising:

fabricating a layer of conductive material;

performing a first etch of the conductive material to define first and second opposite vertical side walls of a gate electrode; and

performing a second etch of the conductive material to form recess regions in the first and second opposite vertical side walls, the recess regions are located at a bottom of the first and second opposite vertical side walls so that a cross-section of the gate electrode generally approximates a T-shape.

14. The method of claim 13 further comprising:

implanting source and drain regions in a substrate which is located below the layer of conductive material, a top of the gate electrode defining lateral boundaries of the source and drain regions so that the source and drain regions are not implanted under the gate electrode.

15. The method of claim 14 further comprising:

thermally processing the source and drain regions to laterally diffuse the source and drain regions under the recess regions of the gate electrode.

16. The method of claim 15 wherein the first etch removes the conductive material to expose a layer of underlaying oxide.

17. The method of claim 15 further comprises performing a third etch to remove residual conductive material remaining after the second etch.

18. The method of claim 13 wherein the recess regions have a lateral depth in the range of 5 to 20 nano meters.

19. A method of reducing overlap capacitance in an integrated circuit transistor, the method comprising:

forming a transistor gate electrode from a single layer of conductive material using an etching process, the gate electrode having a T-shaped cross section;

implanting source and drain regions in a substrate which is located below the gate electrode, a top of the gate electrode defining lateral boundaries of the source and drain regions so that the source and drain regions are not implanted under the gate electrode; and

thermally processing the implanted source and drain regions to laterally diffuse the source and drain regions under the recess regions of the gate electrode.

20. The method of claim 19 wherein the gate electrode has a bottom cross section width that is approximately 20 nano meters less than a top cross section width.

21. The method of claim 19 wherein the transistor gate electrode is formed using a bulk etch process followed by a selective etch process to form bottom side wall notches in the transistor gate electrode.

22. The method of claim 19 wherein the single layer of conductive material is polysilicon.

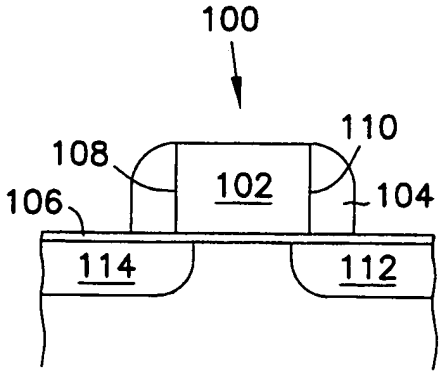

FIG. 1
(PRIOR ART)

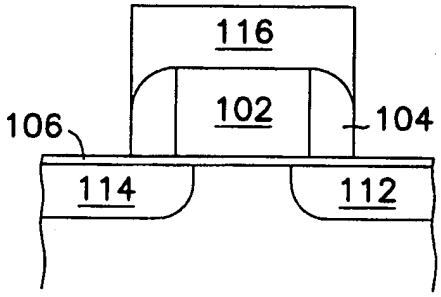

FIG. 2

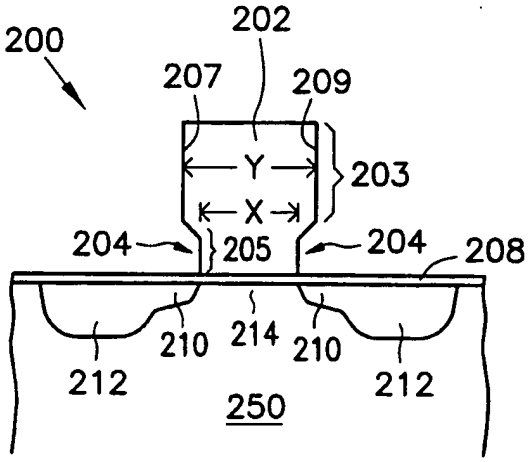

FIG. 3

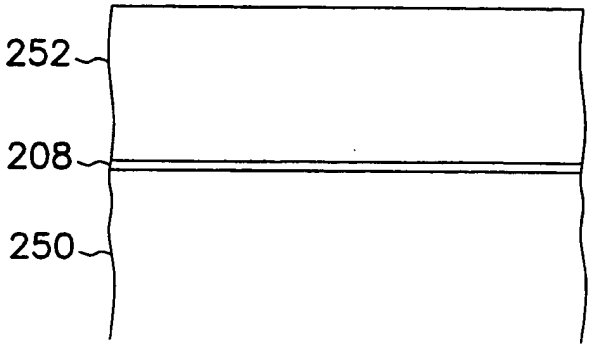

FIG. 4A

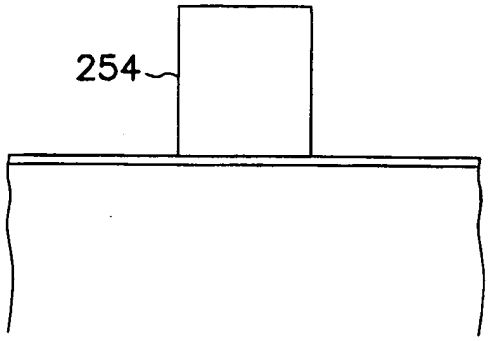

FIG. 4B

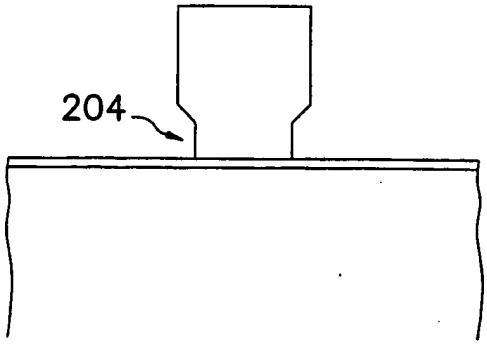

FIG. 4C

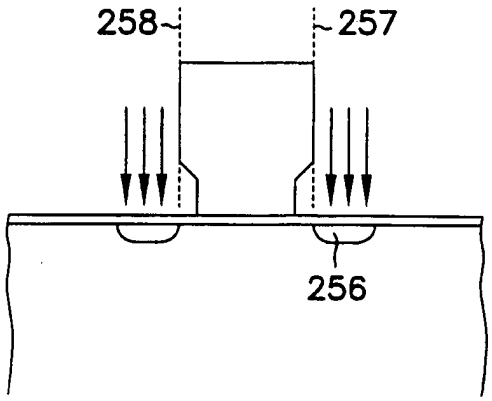

FIG. 4D

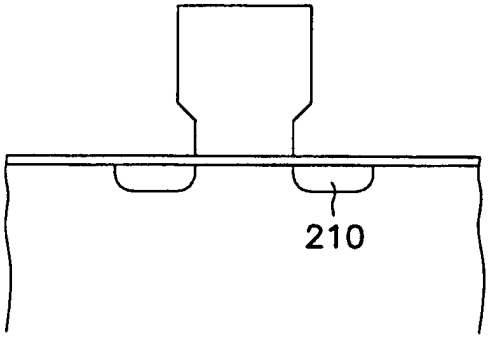

FIG. 4E

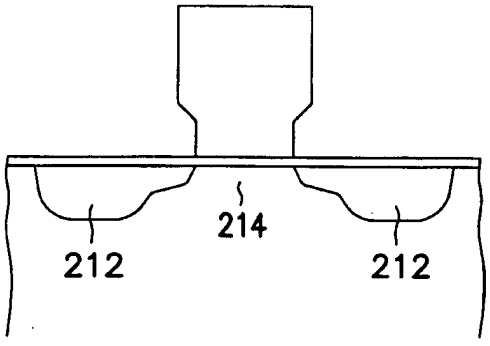

FIG. 4F

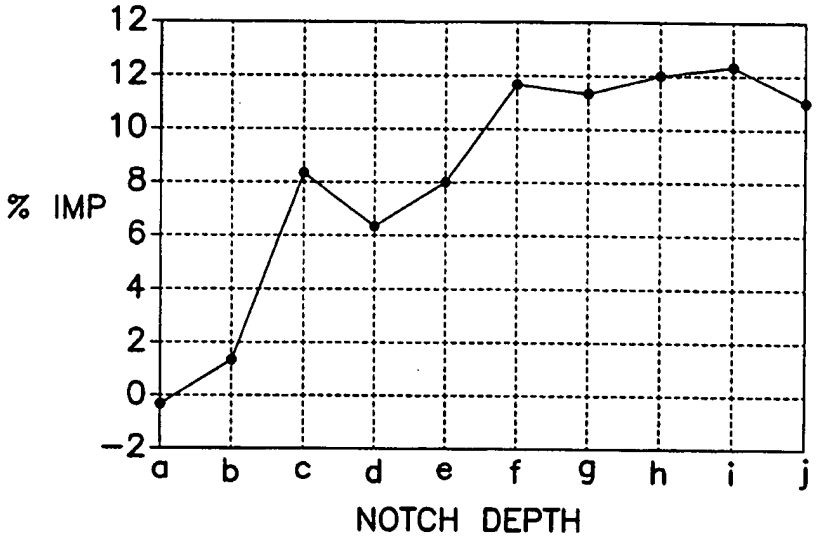

FIG. 5

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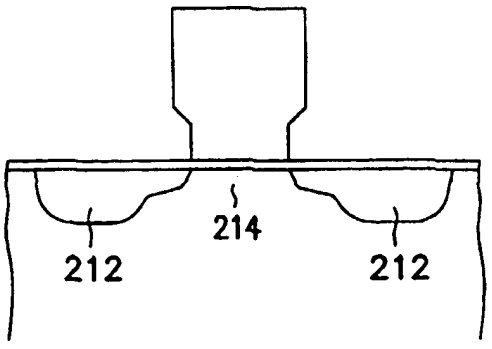
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: TRANSISTOR WITH NOTCHED GATE



(57) Abstract: A transistor having a gate electrode with a T-shaped cross section is fabricated from a single layer of conductive material using an etching process. A two process etch is performed to form sides walls having a notched profile. The notches allow source and drain regions to be implanted in a substrate and thermally processed without creating excessive overlap capacitance with the gate electrode. The reduction of overlap capacitance increases the operating performance of the transistor, including drive current.

WO 00/34984 A3

INTERNATIONAL SEARCH REPORT

Interr plication No
PCT/US 99/29071

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L29/423 H01L21/336 H01L21/28 H01L21/3213

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 834 817 A (EIMORI TAKAHISA ET AL) 10 November 1998 (1998-11-10) column 7, line 10 - line 52; figures 4D,6 column 8, line 63 -column 9, line 47; figure 8	1-22
X	US 5 472 564 A (NAKAMURA MORITAKA ET AL) 5 December 1995 (1995-12-05) column 1, line 17 - line 43; figure 4C column 6, line 33 - line 51	13

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

'A' document defining the general state of the art which is not considered to be of particular relevance

'E' earlier document but published on or after the international filing date

'L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

'O' document referring to an oral disclosure, use, exhibition or other means

'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2000	27/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gélébart, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr Application No
PCT/US 99/29071

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